TECHNICAL REFERENCE

RS-232C 1ch Serial I/O Board for Low Profile PCI

COM-1(LPCI)H

RS-232C 2ch Serial I/O Board for Low Profile PCI

COM-2(LPCI)H

RS-232C 4ch Serial I/O Board for Low Profile PCI

COM-4(LPCI)H

RS-232C 8ch Serial I/O Board for Low Profile PCI

COM-8C-LPCI

Contents

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1. Introduction

This document provides reference concerning I/O port bit allocation as well as the definition of each bit. It is intended for those who are not using our support software or developing applications on non-Windows environment.

1.1. Terminology

Definition of terms:

I/O Base Address
It is the smallest value of I/O resources (I/O range) allocated to a board and is synonymous with top I/O address. Usually, an I/O address of a board means this address.

CH Base Address
The CH base address of each channel is the smallest value of I/O resources (the range of I/O addresses) allocated to that channel, meaning the same as the channel's start address.

2. Product Information

2.1. Vendor ID and Device ID

Information specific to each product is as follows.

Vendor ID : 1221h

Device ID :

Board Name	Device ID
COM-1(LPCI)H	8171h
COM-2(LPCI)H	8181h
COM-4(LPCI)H	8191h
COM-8C-LPCI	9131h

Revision ID : Board ID setup switch (SW1) status. Reflected in the range between 00h and 0Fh.

Technical data excluding those provided above is compliant with PCI local bus specifications.

2.2. Obtaining the Resources

The library for allocating resources (I/O base address, interrupt level, and memory base address) to the PCI bus board in the MS-DOS environment is stored in \Pci\Dos\Samples on the bundled disk "Standard COM Driver Software/COM Setup Disk." Use the library for reference and operation check purposes in your program development.

3. I/O Port Bit Allocation

3.1. I/O Address Map

This board uses the XR16C2850 (manufactured by Exar Corporation) which is upward compatible from the UART 16550.
For details on the internal registers and control of the XR16C2850, refer to the XR16C2850 Data Sheet.

- I/O Port

I/O Base Address	D7	D6	D5	D4	D3	D2	D1	D0
+0h | +7h	Channel 1 register							
+8h | +Fh	Channel 2 register(*1)							
+10h | +17h	Channel 3 register (*1)(*2)							
+18h | +1Eh	Channel 4 register (*1)(*2)							
+1Fh	Interrupt Vector Register 1							
+20h | +27h	Channel 5 register (*1)(*2)(*3)							
+28h | +2Fh	Channel 6 register (*1)(*2)(*3)							
+30h | +37h	Channel 7 register (*1)(*2)(*3)							
+38h | +3Eh	Channel 8 register (*1)(*2)(*3)							
+3Fh	Interrupt Vector Register 2							

(*1)The COM-1(LPCI)H cannot use channel 2 - 8 (+8h - +1Eh, +20h - +3Fh).
(*2)The COM-2(LPCI)H cannot use channel 3 - 8 (+10h - +1Eh, +20h - +3Fh).
(*3)The COM-4(LPCI)H cannot use channel 5 - 8 (+20h - +3Fh).

⚠ CAUTION
Access to each port must be performed in bytes for device specification reasons.
Ports can be accessed only in bytes (neither in words nor in double words).

3.2. Details on I/O Ports and Registers

The XR16C2850's internal registers vary in port map, depending on the value set in the Line Control Register (LCR).
The general registers are enabled either upon startup or unless LCR bit 7 is 0 and the LCR is 0xBF.
The baud registers are enabled when LCR bit 7 is 1.
The enhanced registers are enabled when the LCR is 0xBF.

The CH base address of each channel in the table below is as follows:

CH Base Address of channel 1	I/O Base Address + 0h
CH Base Address of channel 2	I/O Base Address + 8h
CH Base Address of channel 3	I/O Base Address + 10h
CH Base Address of channel 4	I/O Base Address + 18h
CH Base Address of channel 5	I/O Base Address + 20h
CH Base Address of channel 6	I/O Base Address + 28h
CH Base Address of channel 7	I/O Base Address + 30h
CH Base Address of channel 8	I/O Base Address + 38h

- Input Port 1 (General Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	Receive Holding Register (RHR)							
		Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
	+1h	Interrupt Enable Register (IER)							
		CTS Interrupt (*2)	RTS Interrupt (*2)	Xoff Interrupt (*2)	Sleep Mode (*2)	MODEM Status Interrupt	Receive Line Status Interrupt	Transmit Holding Register	Receive Holding Register
	+2h	Interrupt Status Register (ISR)							
		FIFOs Enable	FIFOs Enable	RTS-CTS Change (*2)	Xoff/Special Char (*2)	Int Priority Bit 2	Int Priority Bit 1	Int Priority Bit 0	Int Status
	+3h	Line Control Register (LCR)							
		Divisor Latch Enable	Set Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
	+4h	Modem Control Register (MCR)							
		Clock Prescaler Select (*2)	IR Mode Enable (*2)	Xon Any (*2)	Loop Back Enable	-OP2 and INT Enable	Out 1 0:INT Enable 1:INT Disable (*1)	-RTS	-DTR
	+5h	Line Status Register (LSR)							
		FIFO Error	THR& TSR Empty	THR Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Receive Data Ready
	+6h	Modem Status Register (MSR)							
		-CD	-RI	-DSR	-CTS	Delta -CD	Delta -RI	Delta -DSR	Delta -CTS
	+7h	Scratch Pad Register (SPR) (*4)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+7h	FIFO Level Counter (FLVL) (*3)(*4)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

(*1)For details, see the method of using interrupts.

(*2)This bit is enabled when EFR bit 4 is 1.

(*3)This register is enabled when FCTR bit 6 is 1.

(*4)As the COM-4(LPCI)H uses "+7h (I/O base address + 1Fh) of channel 4" as an interrupt vector register, it can use neither the scratch pad register nor the FIFO level counter of channel 4.

As the COM-8C-LPCI uses "+7h (I/O base address + 1Fh) of channel 4"and "+7h (I/O base address + 3Fh) of channel 8" as an interrupt vector register, it can use neither the scratch pad register nor the FIFO level counter of channel 4 and channel 8.

- Input Port 2 (Baud Rate Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	LSB of Divisor Latch (DLL)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+1h	MSB of Divisor Latch (DLM)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

- Input Port 3 (Enhanced Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	Trigger Level / FIFO Data Count Register							
		Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC
	+1h	Feature Control Register (FCTR)							
		Rx/Tx Mode	SCPAD Swap	Trig Bit 1	Trig Bit 0	RS485 Auto control	IrRx Inv.	-RTS Delay Bit 1	-RTS Delay Bit 0
	+2h	Enhanced Feature Register (EFR)							
		Auto -CTS	Auto -RTS	Special Char, select	Enable IER Bits 4 - 7, ISR, FCR Bits 4 - 5, MCR Bits 5 - 7	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control
	+4h	Xon-1 Word							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+5h	Xon-2 Word							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	+6h	Xoff-1 Word							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+7h	Xoff-2 Word (*1)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

(*1)As the COM-4(LPCI)H uses "+7h (I/O base address + 1Fh) of channel 4" as an interrupt vector register, it can use the xoff-2 word of channel 4. As the COM-8C-LPCI uses "+7h (I/O base address + 1Fh) of channel 4" and "+7h (I/O base address + 3Fh) of channel 8" as an interrupt vector register, it can use the xoff-2 word of channel 4 and channel 8.

- Input Port 4 (Interrupt vector register)

The interrupt vector register of channel 1 - 4 uses "the I/O base address + 1Fh" and that of channel 5 - 8 uses "the I/O base address + 3Fh"

I/O Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+1Fh	Interrupt vector register 1							
		Global interrupt	(Reserved)			CH4 interrupt	CH3 interrupt	CH2 interrupt	CH1 interrupt
	+3Fh	Interrupt vector register 2							
		(Reserved)				CH8 interrupt	CH7 interrupt	CH6 interrupt	CH5 interrupt

- Output Port 1 (General Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	Transmit Holding Register (THR)							
		Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
	+1h	Interrupt Enable Register (IER)							
		CTS Interrupt (*2)	RTS Interrupt (*2)	Xoff Interrupt (*2)	Sleep Mode (*2)	MODEM Status Interrupt	Receive Line Status Interrupt	Transmit Holding Register	Receive Holding Register
	+2h	FIFO Control Register (FCR)							
		RCVR Trigger (MSB)	RCVR Trigger (LSB)	TX Trigger (MSB)	TX Trigger (LSB)	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
	+3h	Line Control Register (LCR)							
		Divisor Latch Enable	Set Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
	+4h	Modem Control Register (MCR)							
		Clock Prescaler Select (*2)	IR Mode Enable (*2)	Xon Any (*2)	Loop Back Enable	-OP2 and INT Enable	Out 1 0:INT Enable 1:INT Disable (*1)	-RTS	-DTR
	+5h	(Not Available)							
	+6h	(Not Available)							
	+7h	Scratch Pad Register (SPR) (*4)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+7h	Enhanced Mode Select Registers (EMSR) (*3) (*4)							
		Reserved	Reserved	RTS Hyst Bit 3	RTS Hyst Bit 2	Reserved	Reserved	Alt.RX/TX FIFO Count	RX/TX FIFO Count

(*1)For details, see the method of using interrupts.

(*2)This bit is enabled when EFR bit 4 is 1.

(*3)This register is enabled when FCTR bit 6 is 1.

(*4)As the COM-4(LPCI)H uses "+7h (I/O base address + 1Fh) of channel 4" as an interrupt vector register, it can use neither the scratch pad register nor the enhanced mode select registers of channel 4.

As the COM-8C-LPCI uses "+7h (I/O base address + 1Fh) of channel 4" and "+7h (I/O base address + 3Fh) of channel 8"as an interrupt vector register, it can use neither the scratch pad register nor the enhanced mode select registers of channel 4 and channel 8.

- Output Port 2 (Baud Rate Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	LSB of Divisor Latch (DLL)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+1h	MSB of Divisor Latch (DLM)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

- Output Port 3 (Enhanced Registers)

CH Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+0h	Trigger Level / FIFO Data Count Register							
		Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC
	+1h	Feature Control Register (FCTR)							
		Rx/Tx Mode	SCPAD Swap	Trig Bit 1	Trig Bit 0	RS485 Auto Control	IrRx Inv.	-RTS Delay Bit 1	-RTS Delay Bit 0
	+2h	Enhanced Feature Register (EFR)							
		Auto -CTS	Auto -RTS	Special Char, Select	Enable IER Bits 4 - 7, ISR, FCR Bits 4 - 5, MCR Bits 5 - 7	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control
	+4h	Xon-1 Word							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+5h	Xon-2 Word							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	+6h	Xoff-1 Word							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	+7h	Xoff-2 Word (*1)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

(*1)As the COM-4(LPCI)H uses "+7h (I/O base address + 1Fh) of channel 4" as an interrupt vector register, it can use the xoff-2 word of channel 4. As the COM-8C-LPCI uses "+7h (I/O base address + 1Fh) of channel 4"and "+7h (I/O base address + 3Fh) of channel 8" as an interrupt vector register, it can use the xoff-2 word of channel 4 and channel 8.

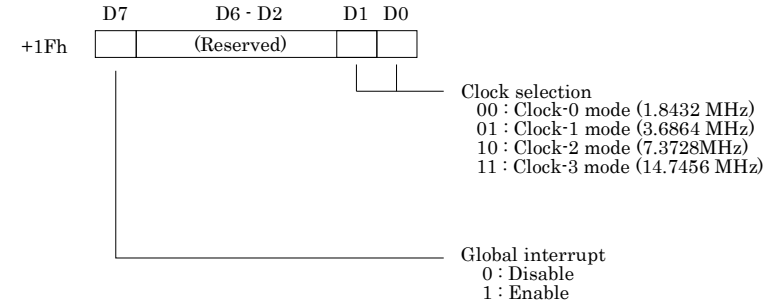
- Output Port 4 (Interrupt Vector Register)

The interrupt vector register uses "the I/O base address + 1Fh" regardless of the channel used.

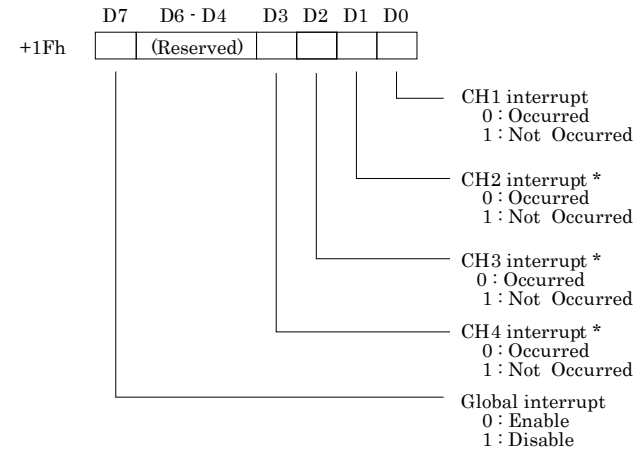
I/O Base Address		D7	D6	D5	D4	D3	D2	D1	D0
	+1Fh	Interrupt Vector Register							
		Global interrupt	(Reserved)					Clock selection Bit 1	Clock selection Bit 0

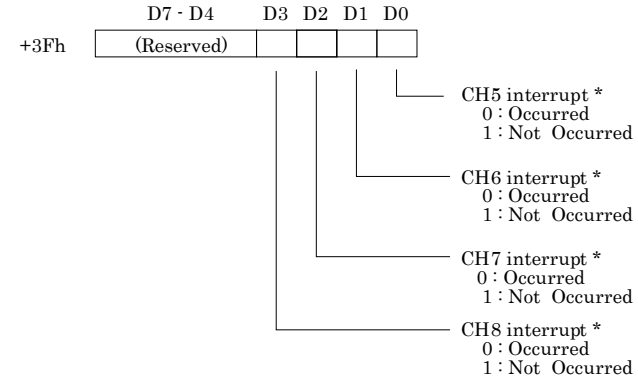
3.3. Interrupt Vector Register

- Output port



- Input port





* The COM-1(LPCI)H cannot use CH2 – CH8 interrupts.
The COM-2(LPCI)H cannot use CH3 – CH8 interrupts.
The COM-4(LPCI)H cannot use CH5 – CH8 interrupts.

4. Operation Procedure

4.1. Access to I/O Ports

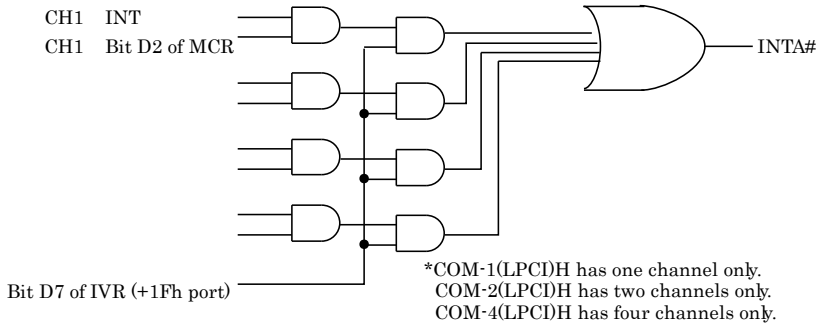
For access to I/O ports, refer to the sample programs stored in \Pci\Dos\Samples on the bundled disk "Standard COM Driver Software/Com Setup Disk."

4.2. Interrupt function

When this board is used, only one interrupt request line is accepted for an interrupt of any of the channels. When an interrupt of each channel is generated, it is latched by the interrupt vector register (IVR). When an interrupt is accepted, the interrupt service routine can identify the channel requesting the interrupt by reading the IVR. When the interrupt service is completed, read the IVR again before leaving the interrupt service to check if any interrupt has been pending.
The XR16C2850 contains a register to enable interrupts by itself and to identify the channel generating an interrupt. For using the register, refer to the data sheet for the XR16C2850 supplied by Exar Corporation.
The board has also a global interrupt to select whether to activate the PCI bus and a selected IRQ line or not.
To use interrupts, enable both of the global interrupt and the interrupt of each channel. Use the D7 bit of the IVR to enable the global interrupt and the D2 bit of the modem control register (MCR) to enable the interrupt of each channel.

Global interrupt (Bit D7 of IVR)	Write "0": Disable (when the power is turned on) Write "1": Enable
Interrupt of each channel (Bit D2 of MCR)	Write "0": Enable (when the power is turned on) Write "1": Disable

Disable interrupts of any channel not to be used.



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