

4ch 32Bit High-Speed Up/Down Counter Board for Low Profile PCI (TTL Input)

CNT32-4MT(LPCI)



* Specifications, color and design of the products are subject to change without notice.

Features

Can input two-phase and single-phase signals.

Can input pulse signals up to 10MHz and can resolve phase differences as short as 25nsec.

Can be converted to a differential input interface using the differential unit (CTP-4D) and connection cable (CNT-68M/50M) which are sold separately.

One control signal input pin per channel.

Can count values sampling at a maximum sampling rate of 20 MHz.

Supporting bus mastering, enabling high-speed data transfer between the board and the PC without intervention from the CPU.

Can generate an interrupt, issuing an external signal, or presetting/zero-clearing the count value when it matches an arbitrary predefined value.

Support for both of low-profile and standard PCI slots (interchangeable with a bundled bracket).

This is a PCI bus compliant interface board for counting the pulses input from the external device.

The board supports a low-profile PCI slot and, if replaced with the supplied bracket, supports a PCI slot, too.

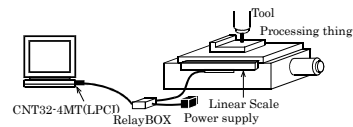
The board has four channels of 32-bit up/down counters, allowing external devices such as a rotary encoder and a linear scale to be connected. Given below are examples of using the board for “detecting a position of the table of a machine tool” and “detecting a change in weight”.

The pulse signal inputting interface is unisolated LVTTTL-level input that can input pulse signals at high speed.

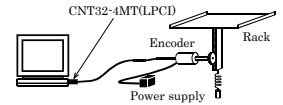
The application for this board can transfer data between the board and the PC at high speed using PCI bus mastering.

<Example >

- Detecting a position of the table of a machine tool



- Detecting a change in weight



Specification

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Item	Specification
Input	
Counter	
Channel count	4 channels
Count system	Up/down counting (2-phase/Single-phase/Single-phase Input with Gate Control Attached)
Max. count	FFFFFFFF(binary data, 32Bit)
Input type	Unisolated LVTTTL level input
Input signal	Phase-A/UP 1 x 4 channels Phase-B/DOWN 1 x 4 channels Phase-Z/CLR 1 x 4 channels
Response frequency	10MHz 50% duty
Digital filter	0.1μsec - 1.6384msec or not used (can be independently set for each channel.)
Timer	1msec - 6553msec 1msec unit
Counter start trigger	Software/External start input/Sampling start trigger
Counter stop trigger	Software/External stop input/Sampling stop trigger
Sampling	
Sampling start trigger	Software/External start input/Count match
Sampling stop trigger	Software/External stop input/Specification number/Bus master transfer error/Count match
Sampling clock	Sampling timer/External clock input
Sampling timer	50nsec - 107sec 25nsec unit(can not be independently set for each channel.)
External sampling start signal	Unisolated LVTTTL level input (Select Rise or Fall)
External sampling stop signal	Unisolated LVTTTL level input (Select Rise or Fall)
External sampling clock signal	Unisolated LVTTTL level input (Fall)
Response frequency	10MHz 50% duty
Control	
Control input signal type	Unisolated LVTTTL level input
Control input channel	1 x 4 channels
Control input signal	- Preset(Select Rise or Fall) - Zero-clear(Select Rise or Fall) - Counter start/stop(Select Rise or Fall) - General-purpose input(positive logic) Software-selected from among the above four options
Response time	100nsec (Max.)
Interrupt event	Count match(8 points), Counter error(2 points), Sampling factor(6 points), Carry/Borrow(1 points), Timer(1 points)

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Item	Specification
Output	
Control	
Control output signal type	Unisolated LVTTTL level output
Control output channel	1 x 4 channels
Control output signal	- Count match 0 output(one-shot pulse output) - Count match 1 output(one-shot pulse output) - Digital filter error output(one-shot pulse output) - Abnormal input error output(one-shot pulse output) - General-purpose output(Level output) Software-selected from among the above five options (Positive/negative logic is selected with the software.)
One shot output signal amplitude	Selected between 10 μ sec, 100 μ sec, 1msec, 10msec and 100 msec (Can be set for each channel, within precision + 1 μ sec)
Response time	100nsec (Max.)
Rated output current	I _{OL} =8mA(Max.) I _{OH} =-8mA(Max.)
Test pulse	
Test pulse output signal type	Unisolated LVTTTL level output
Test pulse output point	One for each of phases-A and B
Output frequency	100kHz fixed
Sampling	
Sampling output signal type	Unisolated LVTTTL level output
Output point	Sampling start trigger, sampling stop trigger, Sampling clock trigger 1 point each
One-shot output signal width	Negative logic 100nsec (fixed)
Response speed	100nsec (Max.)
Rated output current	I _{OL} = 8mA(Max.) I _{OH} = -8mA(Max.)
Bus master	
DMA channel	1 channel
Transfer bus width	32-Bit width
Transfer data length	8 PCI Words length(Max.)
Transfer rate	80MB/sec(Max.133MB/sec)
FIFO	1K-DWord
Scatter/Gather function	64MB
Interrupt event	Bus master event(7 points)
Common	
I/O address	Occupies 2 locations, any 32-bytets and 64-byte boundary
Power consumption	5VDC 300mA (Max.)
Operating condition	0 - 50°C, 10 - 90%RH (No condensation)
PCI bus specification	33bit, 33MHz, Universal key shapes supported *1
Dimension (mm)	121.69(L) x 63.41 (H)
Weight	60g
Standard	VCCI Class A, CE Marking (EMC Directive Class A, RoHS Directive), UKCA

*1 This board requires power supply at +5 V from an expansion slot (it does not work on a machine with a +3.3-V power supply alone).

Support Software

The name of the documents	Contents	How to get
Counter Driver API-CNT(WDM)	Driver software of counter input	Download (ZIP)

* Download the software from the CONTEC website.

Cable & Connector

Cable(Optional)

Shielded cable for CardBus counter input card
: CNT-68M/50M (0.5m)

Cable with 68-Pin D-sub Connector
at either Ends (Mold Type) : PCB68PS-0.5P (0.5m)
: PCB68PS-1.5P (1.5m)

Shielded cable with single connector
for 68-pin 0.8mm pitch connector : PCA68PS-0.5P (0.5m)
: PCA68PS-1.5P (1.5m)

Accessories

Accessories (Option)

Termination Panel with Differential Receivers
for Counter Input : CTP-4D *1
Screw Terminal (M3 x 50P) : EPD-50A *1*3
Screw Terminal (M3 x 68) : EPD-68A *2*3

*1 CNT-68M/50M optional cable is required separately.

*2 PCB68PS-0.5P or PCB68PS-1.5P optional cable is required separately.

*3 "Spring-up" type terminal is used to prevent terminal screws from falling off.

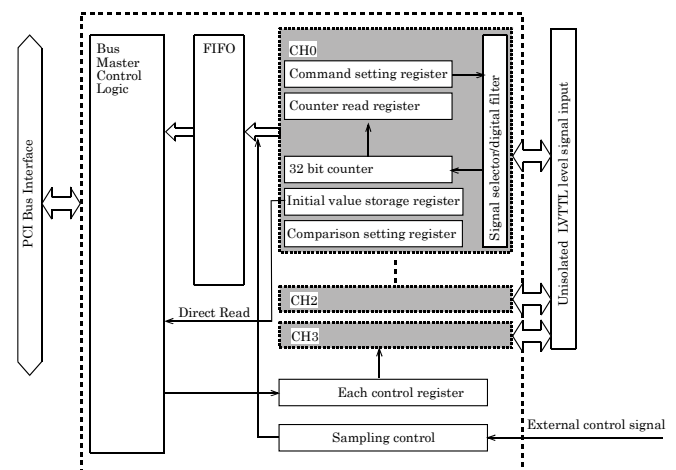
* Check the CONTEC's Web site for more information on these options.

Packing List

Board [CNT32-4MT(LPCI)] ...1
First step guide ... 1
CD-ROM *1 [API-PAC(W32)] ...1
Bracket for PCI...1

*1 The CD-ROM contains the driver software and User's Guide.

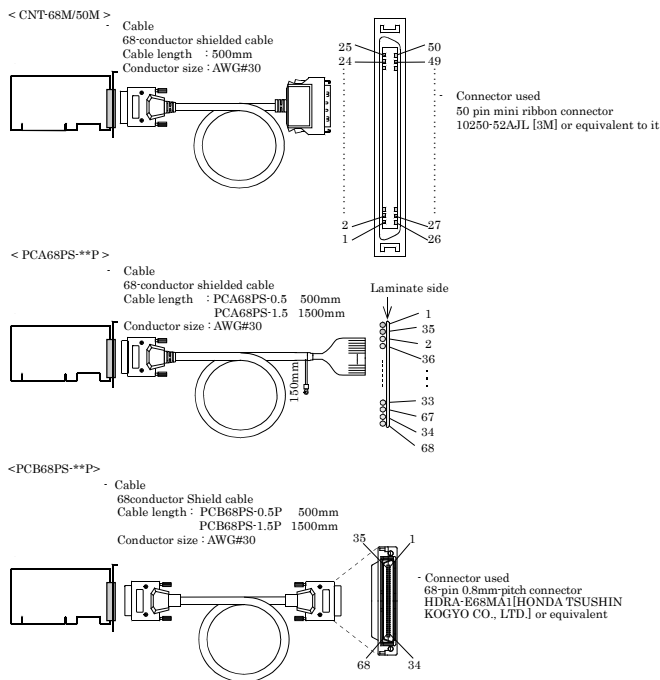
Block Diagram



Using the On- Board Connectors

Connecting a Board to a Connector

Use the optional connection cable (CNT-68M/50M or PCA68PS-**P, PCB68PS-**P) to connect the board to an external device. Uses the cable together with a terminal block for the wiring between the board and external device.



Connector Pin Assignment

Pin Assignment of an interface connector(CN1)(Board side)

CH0 Phase-A input	A0	1	35	- GND	Ground
CH0 Phase-B input	B0	2	36	- GND	Ground
CH0 Phase-Z input	Z0	3	37	- GND	Ground
CH0 control input *1	D10	4	38	- GND	Ground
Unconnection	N.C.	5	39	- N.C.	Unconnection
CH1 Phase-A input	A1	6	40	- GND	Ground
CH1 Phase-B input	B1	7	41	- GND	Ground
CH1 Phase-Z input	Z1	8	42	- GND	Ground
CH1 control input *1	D11	9	43	- GND	Ground
Unconnection	N.C.	10	44	- N.C.	Unconnection
CH2 Phase-A input	A2	11	45	- GND	Ground
CH2 Phase-B input	B2	12	46	- GND	Ground
CH2 Phase-Z input	Z2	13	47	- GND	Ground
CH2 control input *1	D12	14	48	- GND	Ground
Unconnection	N.C.	15	49	- N.C.	Unconnection
CH3 Phase-A input	A3	16	50	- GND	Ground
CH3 Phase-B input	B3	17	51	- GND	Ground
CH3 Phase-Z input	Z3	18	52	- GND	Ground
CH3 control input *1	D13	19	53	- GND	Ground
Unconnection	N.C.	20	54	- N.C.	Unconnection
Sampling clock input	CLKIN	21	55	- GND	Ground
Sampling stop input	STOPIN	22	56	- STARTIN	Sampling start input
Unconnection	N.C.	23	57	- N.C.	Unconnection
Sampling clock output	CLKOUT	24	58	- GND	Ground
Sampling stop output	STOPOUT	25	59	- STARTOUT	Sampling start output
Unconnection	N.C.	26	60	- N.C.	Unconnection
Test pulse Phase-A output	TPOA	27	61	- TPOB	Test pulse Phase-B output
Unconnection	N.C.	28	62	- N.C.	Unconnection
CH0 control output *2	DO0	29	63	- DO1	CH1 control output *2
CH2 control output *2	DO2	30	64	- DO3	CH3 control output *2
Unconnection	N.C.	31	65	- N.C.	Unconnection
Counter input signal pull up	PUP1	32	66	- PUP2	Control input signal pull up
Unconnection	N.C.	33	67	- N.C.	Unconnection
+3.3V output *3	Vcc	34	68	- Vcc	+3.3V output *3

*1 The control input can serve as the general-input, counter start/stop, preset, and zero-clear.

*2 The control output can serve as the general-output, count match, abnormal input error and digital filter error.

*3 Supply-capable current is 500mA (Max.).

Pin Assignment of CNT-68M/50M

+3.3V Output *3	Vcc	25	50	- Vcc	+3.3V Output *3
Counter Input signal pull-up	PUP1	24	49	- PUP2	Counter Input signal pull-up
CH2 control output *2	DO2	23	48	- DO3	CH3 control output *2
CH0 control output *2	DO0	22	47	- DO1	CH1 control output *2
Test pulse Phase-A output	TPOA	21	46	- TPOB	Test pulse Phase-B output
Sampling Stop Output	STOPIN	20	45	- STARTOUT	Sampling Start Output
Sampling Clock Output	CLKOUT	19	44	- GND	Ground
Sampling Stop Input	STOPIN	18	43	- STARTIN	Sampling Start Input
Sampling Clock Input	CLKIN	17	42	- GND	Ground
CH3 Control Input *1	D13	16	41	- GND	Ground
CH3 Phase-Z input	Z3	15	40	- GND	Ground
CH3 Phase-B input	B3	14	39	- GND	Ground
CH3 Phase-A input	A3	13	38	- GND	Ground
CH2 Control Input *1	D12	12	37	- GND	Ground
CH2 Phase-Z input	Z2	11	36	- GND	Ground
CH2 Phase-B input	B2	10	35	- GND	Ground
CH2 Phase-A input	A2	9	34	- GND	Ground
CH1 Control Input *1	D11	8	33	- GND	Ground
CH1 Phase-Z input	Z1	7	32	- GND	Ground
CH1 Phase-B input	B1	6	31	- GND	Ground
CH1 Phase-A input	A1	5	30	- GND	Ground
CH0 Control Input *1	D10	4	29	- GND	Ground
CH0 Phase-Z input	Z0	3	28	- GND	Ground
CH0 Phase-B input	B0	2	27	- GND	Ground
CH0 Phase-A input	A0	1	26	- GND	Ground

*1 The control input can serve as the general-input, counter start/stop, preset, and zero-clear.

*2 The control output can serve as the general-output, count match, abnormal input error and digital filter error.

*3 Supply-capable current is 500mA (Max.).

How to Connect the Counter Input Signal

You can connect to a rotary encoder or linear scale with a TTL level output circuit, or to an open-collector output circuit. The signal must be an LVTTTL level input and can be up to 10MHz.

As pull-up resistors are provided on the board, connect the pull-up voltage (3.3V to 5.5V max.) to the pull-up pins if connecting to an open collector output circuit/TTL-level output circuit. (If using 3.3V, connect to the VCC pin on the board.) Not connecting the pull-up voltage may affect the counter input channel left unconnected.

For a two-phase input, connect both phase A and phase B. For a single phase input, connect to either phase A or phase B. If not using the Z phase, this does not need to be connected.

Remarks

The pull-up pins are PUP1 (pin 32 *1) for the counter input signal and PUP2 (pin 66 *1) for the control input signal.

PUP1 (pin 32):

Pull-up for A, B, and Z phase input signal (A0, B0, Z0, A1, B1, Z1, A2, B2, Z2, A3, B3, Z3).

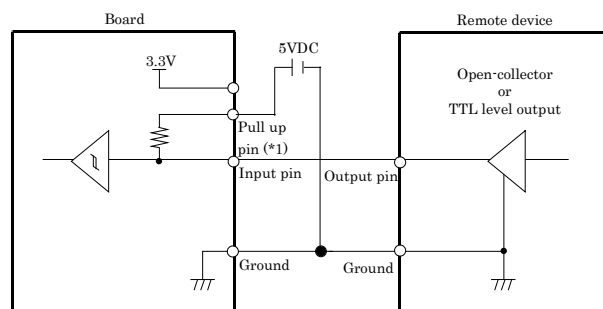
PUP2 (pin 66):

Pull-up for the control input signals and for the sampling input signals (DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN).

*1 Connector pin number on the board.

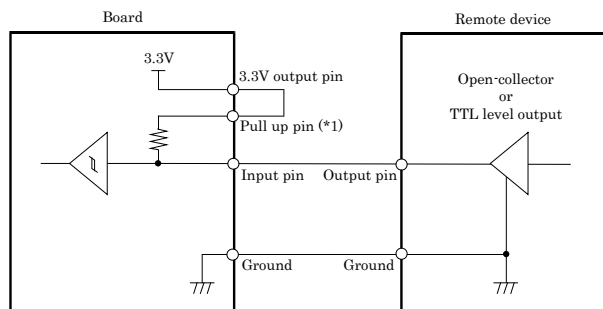
Example Connection for Counter Input Circuit

Connection pulled up with external 5-V power (Counter Input)



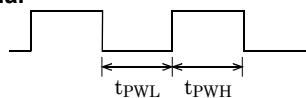
*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Connection pulled up with internal 3.3-V output power (Counter Input)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Input signal



tpWH : High-level count input pulse width 50nsec (Min.)

tpWL : Low-level count input pulse width 50nsec (Min.)

CAUTION

The connection cable length should be within 1.5 m.

To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.

Connecting the control signal input/output

Connection of a control input

The control input signals consist of one pin per channel that can be selected as the channel's counter start/stop or preset, and one pin per board that can be used as the start, stop, and clock for sampling. The signals are LVTTTL-level inputs.

As pull-up resistors (10K Ω) are provided on the board, connect the pull-up voltage (3.0V to 5.5V max.) to the pull-up pins if connecting to an open collector output circuit/TTL-level output circuit. (If using 3.3V, connect to the VCC pin on the board.) Not connecting the pull-up voltage may affect the control input pin left unconnected.

Remarks

The pull-up pins are PUP1 (pin 32 *1) for the counter input signal and PUP2 (pin 66 *1) for the control input signal.

PUP1 (pin 32):

Pull-up for A, B, and Z phase input signal (A0, B0, Z0, A1, B1, Z1, A2, B2, Z2, A3, B3, Z3).

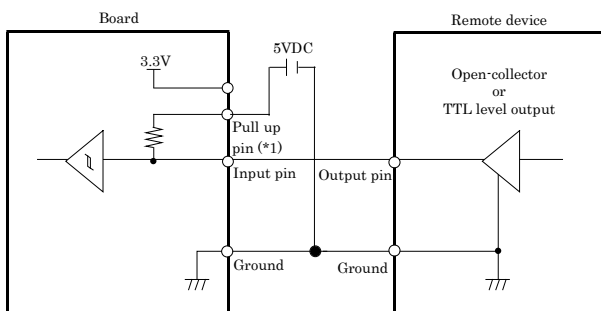
PUP2 (pin 66):

Pull-up for the control input signals and for the sampling input signals (DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN).

*1 Connector pin number on the board.

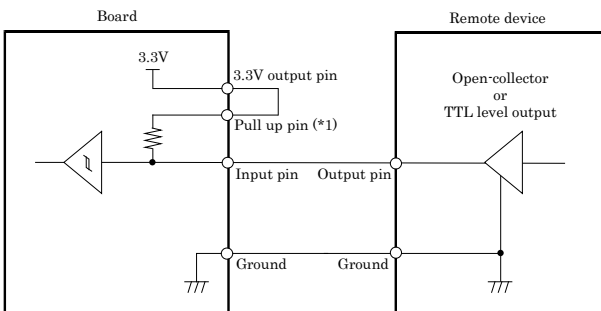
Control input circuit and its sample connection

Connection pulled up with external 5-V power (Control input DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Connection pulled up with internal 3.3-V output power (Control input DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

CAUTION

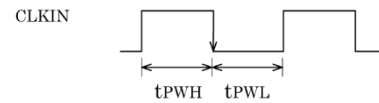
The connection cable length should be within 1.5 m.

To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.

External sampling clock signal (CLKIN)

Pin used to input the external pacer clock. The maximum frequency is 10MHz.

If the external clock input is selected as the sampling clock, sampling occurs on the falling edge of the signal.



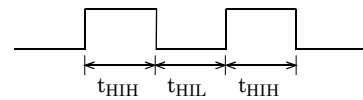
tPWH : High-level clock pulse width 50nsec (Min.)

tPWL : Low-level clock pulse width 50nsec (Min.)

Other control input signals

(DI0 to DI3, STARTIN, STOPIN)

These signals are TTL-level compatible and the trigger edge is software-programmable at either the rising or falling edge. High- and low-level hold times of at least 50 nsec are required to detect an edge of the signal.



tHIL : High-level hold time 50nsec (Min.)

tHIL : Low-level hold time 50nsec (Min.)

Connection of a control output

This outputs a general-purpose output signal (level output) or a one-shot pulse output to indicate a hardware event such as a count match. The signal is an LVTTTL level output and can be set to positive or negative logic by software.

Control output circuit and its sample connection

