8ch 32Bit Up/Down High-Speed Counter Board for PCI

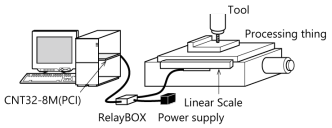
CNT32-8M(PCI)

* Specifications, color and design of the products are subject to change without notice.

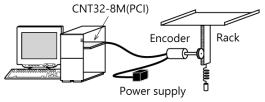
This product is a PCI bus-compliant interface board that counts input pulse signals from external devices.
This product has eight channels of 32-bit up/down counters, allowing external devices such as a rotary encoder and a linear scale to be connected.
Given below are examples of using the board for "detecting a position of the table of a machine tool" and "detecting a change in weight".
The pulse signal incoming interface is differential line receiver input or TTL level -compatible input that can receive pulse signals at high speed.
Windows/Linux device driver is supported with this product.

< Example >

- Detecting a position of the table of a machine tool



- Detecting a change in weight



* The contents in this document are subject to change without notice.
* Visit the CONTEC website to check the latest details in the document.
* The information in the data sheets is as of November, 2024.

Features

8ch 32-bit up/down counter, high speed pulse input of 10MHz, and disconnection detection are available.

A 32-bit up/down counter with 8 channels is mounted on one board, high speed pulse input up to 10MHz (unisolated TTL-level input, differential line receiver) is available, and disconnection detection can be performed for differential line receiver input.

2-phase signals and 1-phase signals such as a rotary encoder or linear scale can be counted. Surge protection is realized by implementing protectors in the input circuit.

In addition, 1pin/ch of control input signal is provided. It can be used as counter start/stop, preset, zero clear, general-purpose input.

Bus master transfer function is provided.

Bus master transfer makes it possible to transfer large data at a high speed without extra CPU load.

Digital filter function to prevent wrong recognition of input signals due to noises is provided.

Digital filter function by which noises of counter input signals (phase-A, phase-B, phase-Z) and control input signals can be prevented is equipped. Digital filter can either be not used or set within the range of 0.1µ - 1.6384msec by software.

In addition, as all these input signals are taken into the internal counter via the digital filter, when using the digital filter, these signals are taken in with a delay of a specified duration.

Windows/Linux support device driver

Using the device driver API-TOOL makes it possible to create applications of Windows/Linux. In addition, a diagnostic program by which the operations of hardware can be checked is provided.

The synchronization control connectors are provided

The synchronization control connectors which can make boards up to 16 pieces synchronously run are provided. In addition, the synchronous operation with CONTEC boards where a synchronization control connector is mounted can be easily realized.

The input circuit has a built-in varistor for voltage surge protection

To protect the input circuit from voltage surges, a varistor is connected.

Independent general-purpose timer is provided

The timer which can let interrupts occur at a specified interval is provided.

The timer can be set within the range of 1 - 6553msec (selectable in step of 1 msec).

Specifications

Function specification

Item	Specifications
Input	
Counter	
Channel count	8 channels
Count system	Up/down counting (2-phase/Single-phase/Single-phase Input with Gate Control Attached)
Max. count	FFFFFFFFh (binary data, 32Bit)
Input type	Differential line receiver input or TTL level input (Selectable by software)
Input signal	Phase-A/UP One x 8 channels Phase-B/DOWN One x 8 channels Phase-Z/CLR One x 8 channels
Differential line receiver input section	Element in use: Equivalent to AM26LS32 (T.I) Terminating resistance: 150Ω (Can be disconnected switch.) Receiver input sensitivity: ±200mV In-phase input voltage range: 0 - +7V Signal extension distance: 1200m (dependent on wiring environment and input frequency) *1*2
TTL level input section *3	Element in use: Equivalent to 74ALS541NS (T.I) Signal extension distance: 1.5m (dependent on wiring environment)
Response frequency	10MHz 50% duty
Digital filter	0.1µsec - 1.6384msec or not used (can be independently set for each channel.)
Timer	1msec - 6553msec 1msec unit
Counter start trigger	Software/External start input/Sampling start trigger
Counter stop trigger	Software/External start input/Sampling stop trigger
Sampling *3	
Sampling start trigger	Software/External start input/Sync control connectors/Count match
Sampling stop trigger	Software/External stop input/Specification number/Bus master transfer error/Sync control connectors/Count match
Sampling clock	Sampling timer/External clock input/Sync control connectors
Sampling timer	50nsec - 107sec 5nsec unit (can not be independently set for each channel.)
External sampling start signal	TTL level (Select Rise or Fall)
External sampling stop signal	TTL level (Select Rise or Fall)
External sampling clock signal	TTL level (Fall)
Response frequency	10MHz 50% duty
Control *3	
Control input signal type	TTL level
Control input channel	One x 8 channels
Control input signal	- Preset (Select Rise or Fall) - Zero-clear (Select Rise or Fall) - Counter start/stop (Select Rise or Fall) - General-purpose input (positive logic) Software-selected from among the above four options

Item		Specifications
	Response time	100nsec (Max.)
Interrupt event		Count match (16 points), Counter error (2 points), Sampling factor (6 points), Sync control connectors error (2 points), Carry/Borrow (1 points), Timer (1 points)
Output *3		
Control		
	Control output channel	One x 8 channels
	Control output signal	- Count match 0 output (one-shot pulse output) - Count match 1 output (one-shot pulse output) - Digital filter error output (one-shot pulse output) - Abnormal input error output (one-shot pulse output) - Disconnection alarm error output (one-shot pulse output) - General-purpose output (Level output) Software-selected from among the above five options (Positive/negative logic is selected with the on-board switch.)
	One shot output signal amplitude	Selected between 10µsec, 100µsec, 1msec, 10msec and 100 msec (Can be set for each channel, within precision + 1µsec)
	Element in use	Non-Isolated Open Collector Output: Equivalent to 74LS07NS(T.I)
	Output rating	30V 40mA
	Response speed	5µsec (Max.)
TP		
	Test pulse output signal	One line receiver output for each of phases-A and B (For TTL output, use the positive line receiver output.)
	Element in use	AM26LS31(T.I) or Equivalent
	Frequency	100kHz
Bus master		
DMA channel		1 channel
Transfer bus width		32-Bit width
Transfer data length		8 PCI Words length (Max.)
Transfer rate		80MB/sec (Max.133MB/sec)
FIFO		1K-DWord
Scatter/Gather function		64MB
Interrupt event		Bus master event (7 points)
Synchronization		
Control output signal		Select the output signal by software when setting the synchronization slave mode.
Control input signal		Select the synchronization event by software when setting the synchronization slave mode.
Connectable number of device		16 boards including the master board
Connector used		PS-10PE-D4T1-B1 (JAE) or equivalent x 2
Common		
I/O address		Occupies 2 locations, any 32-bytets and 64-byte boundary
Power consumption		5VDC 1A (Max.)
PCI bus specification		32bit, 33MHz, Universal key shapes supported *4
Dimension (mm)		176.41(L) x 106.68(H)
Weight		120g

*1 The frequency response at an extension of 50 m is about 10 MHz (depending on the wiring environment).
The frequency response at an extension of 100 m is about 5 MHz (depending on the wiring environment).
The frequency response at an extension of 150 m is about 1.5 MHz (depending on the wiring environment).
The frequency response at an extension of 300 m is about 1 MHz (depending on the wiring environment).
The frequency response at an extension of 600 m is about 500 KHz (depending on the wiring environment).
The frequency response at an extension of 1200 m is about 80 KHz (depending on the wiring environment)

*2 Please use the shielded cable with a length of less than 30m to meet "CE EMC Directive".

*3 Please use the shielded cable to meet "CE EMC Directive".

*4 This board requires power supply at +5V from an expansion slot (it does not work on a machine with a +3.3V power supply alone).

Installation Environment Requirements

Item	Specifications
Operating ambient temperature	0 - 50℃
Operating ambient humidity	10 - 90%RH (No condensation)
Floating dust particles	Not to be excessive
Corrosive gases	None
Standard	VCCI Class A, CE Marking (EMC Directive Class A, RoHS Directive), UKCA

Difference in bus mastering transfer rate by system configuration

When it inserts in the expansion slot of a personal computer

	Limited	Unlimited
430TX/Pentium233MHz	20	13.4
440BX/PentiumII450MHz	20	13.4
i820/PentiumIII800MHz	20	13.4
i815E/PentiumIII800MHz	20	13.4

[MHz]

"Limited" indicates that the number of transfers is specified; "Unlimited" specifies that it is not specified. These values may not be satisfied depending on the system configuration including other boards and applications.

When CONTEC's extension unit FA-PAC(PCI) series is used

	Limited	Unlimited
430TX/Pentium233MHz	20	10
440BX/PentiumII450MHz	20	10
i820/PentiumIII800MHz	20	10
i815E/PentiumIII800MHz	20	10

[MHz]

"Limited" indicates that the number of transfers is specified; "Unlimited" specifies that it is not specified. These values may not be satisfied depending on the system configuration including other boards and applications.

Support Software

Name	Contents	How to get
Windows Version Counter Driver software API-CNT(WDM)	The Windows device driver is provided as a form of Windows API functions. Various sample programs such as C# and Visual Basic .NET , Visual C++, Python etc. and diagnostic program useful for checking operation is provided.	Download from the CONTEC website *1
Linux Version Counter Driver software API-CNT(LNX)	The Linux device driver is provided as a shared library. The software includes various sample programs such as gcc (C, C++) and Python programs, as well as a configuration tool to configure the device settings.	Download from the CONTEC website *1
Software Development Tool Kits (SDK) and Support Software	In addition to the device drivers, we offer many software programs for using CONTEC devices in an easier manner.	Download from the CONTEC website *2

*1 Download the files from the following URL.
https://www.contec.com/download/

*2 For supported software, search the CONTEC website for this product and view the product page.
https://www.contec.com/

Optional Products

Product Name	Model type	Description
Shielded Cable with Two 96-Pin Half-Pitch Connectors	PCB96PS-0.5P	0.5m
	PCB96PS-1.5P	1.5m
Flat Cable with 96-pin Half-Pitch Connectors at Both Ends	PCB96P-1.5	1.5m
Shielded Cable with One 96-pin Half-Pitch Connector	PCA96PS-0.5P	0.5m
	PCA96PS-1.5P	1.5m
Flat Cable with One 96-pin Half-Pitch Connector	PCA96P-1.5	1.5m
Screw Terminal (M3 * 96)	EPD-96A	*1 *2
Terminal Unit for Relay Terminal Banks	EPD-96	*2
Screw Terminal	DTP-64A	*2

*1 "Spring-up" type terminal is used to prevent terminal screws from falling off.

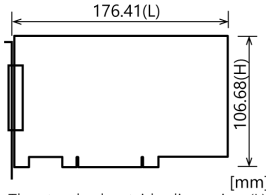
*2 PCB96P or PCB96PS optional cable is required separately.

Visit the CONTEC website for the latest optional products.

Included Items

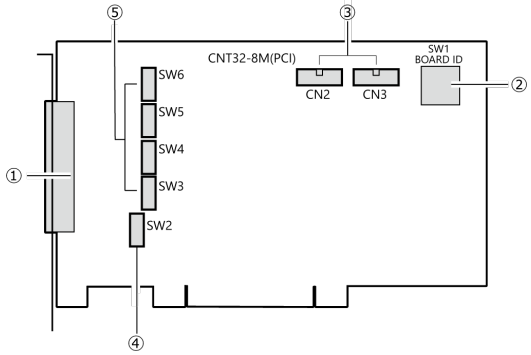
Product [CNT32-8M(PCI)] ...1
Synchronization Control Cable (10cm) ... 1
Please read the following ... 1

Physical Dimensions



The standard outside dimension (L) is the distance from the end of the board to the outer surface of the slot cover.

Nomenclature of Product Components

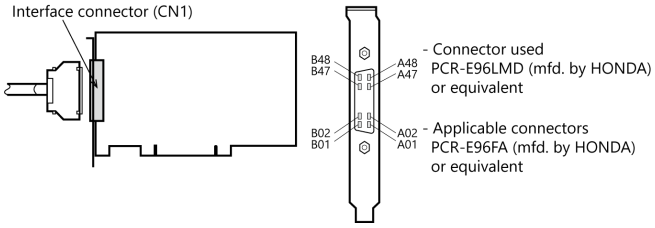


No.	Name	No.	Name
1	Interface Connector (CN1)	4	Switch for setting output signal logic (SW2)
2	Board ID Setting Switch (SW1)	5	Switch for setting terminator (SW3, SW4, SW5)
3	Synchronous control connector (CN2, CN3)		

Connecting to an External Device

Connecting an Interface Connector

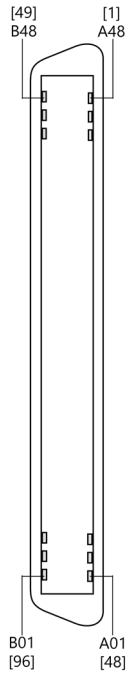
To connect an external device to this product, plug the cable from the device into the interface connector (CN1) shown below.



Signal Layout of CNT32-8M(PCI) Interface Connector

Layout on the Interface Connector (CN1)

Ground	GND	B48		A48	GND	Ground
	GND	B47		A47	GND	
CH7 differential Phase-Z	D7Z-	B46		A46	D3Z-	CH3 differential Phase-Z input -
CH7 TTL Phase-Z input/ Differential Phase-Z input+	T7Z/D7Z+	B45		A45	D3Z+/T3Z	CH3 differential Phase-Z input+/ TTL Phase-Z input
CH7 differential Phase-B input-	D7B-	B44		A44	D3B-	CH3 differential Phase-B input-
CH7 TTL Phase-B input/ Differential Phase-B input+	T7B/D7B+	B43		A43	D3B+/T3B	CH3 differential Phase-B input+/ TTL Phase-B input
CH7 differential Phase-A input-	D7A-	B42		A42	D3A-	CH3 differential Phase-A input-
CH7 TTL Phase-A input/ Differential Phase-A input+	T7A/D7A+	B41		A41	D3A+/T3A	CH3 differential Phase-A input+/ TTL Phase-A input
Ground	GND	B40		A40	GND	Ground
	GND	B39		A39	GND	
CH6 differential Phase-Z input-	D6Z-	B38		A38	D2Z-	CH2 differential Phase-Z input-
CH6 TTL Phase-Z input/ Differential Phase-Z input+	T6Z/D6Z+	B37		A37	D2Z+/T2Z	CH2 differential Phase-Z input+/ TTL Phase-Z input
CH6 differential Phase-B input-	D6B-	B36		A36	D2B-	CH2 differential Phase-B input-
CH6 TTL Phase-B input/ Differential Phase-B input+	T6B/D6B+	B35		A35	D2B+/T2B	CH2 differential Phase-B input+/ TTL Phase-B input
CH6 differential Phase-A input-	D6A-	B34		A34	D2A-	CH2 differential Phase-A input-
CH6 TTL Phase-A input/ Differential Phase-A input+	T6A/D6A+	B33		A33	D2A+/T2A	CH2 differential Phase-A input+/ TTL Phase-A input
Ground	GND	B32		A32	GND	Ground
	GND	B31		A31	GND	
CH5 differential Phase-Z input-	D5Z-	B30		A30	D1Z-	CH1 differential Phase-Z input-
CH5 TTL Phase-Z input/ Differential Phase-Z input+	T5Z/D5Z+	B29		A29	D1Z+/T1Z	CH1 differential Phase-Z input+/ TTL Phase-Z input
CH5 differential Phase-B input-	D5B-	B28		A28	D1B-	CH1 differential Phase-B input-
CH5 TTL Phase-B input/ Differential Phase-B input+	T5B/D5B+	B27		A27	D1B+/T1B	CH1 differential Phase-B input+/ TTL Phase-B input
CH5 differential Phase-A input-	D5A-	B26		A26	D1A-	CH1 differential Phase-A input-
CH5 TTL Phase-A input/ Differential Phase-A input+	T5A/D5A+	B25		A25	D1A+/T1A	CH1 differential Phase-A input+/ TTL Phase-A input
Ground	GND	B24		A24	GND	Ground
	GND	B23		A23	GND	
CH4 differential Phase-Z input-	D4Z-	B22		A22	D0Z-	CH0 differential Phase-Z input-
CH4 TTL Phase-Z input/ Differential Phase-Z input+	T4Z/D4Z+	B21		A21	D0Z+/T0Z	CH0 differential Phase-Z input+/ TTL Phase-Z input
CH4 differential Phase-B input-	D4B-	B20		A20	D0B-	CH0 differential Phase-B input-
CH4 TTL Phase-B input/ Differential Phase-B input+	T4B/D4B+	B19		A19	D0B+/T0B	CH0 differential Phase-B input+/ TTL Phase-B input
CH4 differential Phase-A input-	D4A-	B18		A18	D0A-	CH0 differential Phase-A input-
CH4 TTL Phase-A input/ Differential Phase-A input+	T4A/D4A+	B17		A17	D0A+/T0A	CH0 differential Phase-A input+/ TTL Phase-A input
Ground	GND	B16		A16	GND	Ground
	GND	B15		A15	GND	
CH7 control input *1	DI7	B14		A14	DI3	CH3 control input *1
CH6 control input *1	DI6	B13		A13	DI2	CH2 control input *1
CH5 control input *1	DI5	B12		A12	DI1	CH1 control input *1
CH4 control input *1	DI4	B11		A11	DI0	CH0 control input *1
External sampling start signal input	EXTSTART	B10		A10	EXTCLK	External sampling clock input
External sampling stop signal input	EXTSTOP	B09		A09	GND	Ground
Ground	GND	B08		A08	GND	
CH7 control output *2	DO7	B07		A07	DO3	CH3 control output *2
CH6 control output *2	DO6	B06		A06	DO2	CH2 control output *2
CH5 control output *2	DO5	B05		A05	DO1	CH1 control output *2
CH4 control output *2	DO4	B04		A04	DO0	CH0 control output *2
Ground	GND	B03		A03	GND	Ground
Test pulse differential Phase-A output-	TPOA-	B02		A02	TPOB-	Test pulse differential Phase-B output-
Test pulse TTL Phase-A output/ Differential Phase-A output+	TPOA+	B01		A01	TPOB+	Test pulse differential Phase-B output+/TTL Phase-B output



* The numbers in square brackets [ ] are pin numbers designated by HONDA TSUSHIN KOGYO CO., LTD.

*1 The control inputs can serve as the general-purpose, counter start/stop, preset, and zero-clear inputs.

*2 The control outputs can serve as the general-purpose output, count match, abnormal input error, digital filter error, and discontinuity alarm error outputs.

Connection Method to the External device -Differential Input-

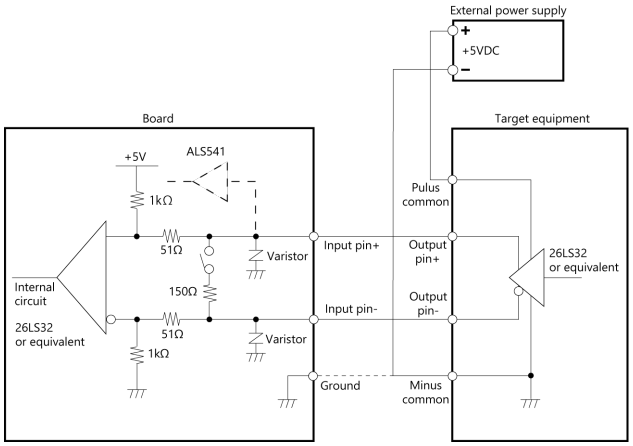
Differential Input Connection

Use the differential line receiver input to connect the board to the line receiver output circuit of a rotary encoder or linear scale. The maximum input frequency is 10 MHz.

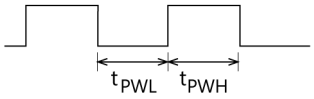
For use in two-phase input mode, connect both of the phase-A and phase-B inputs. For use in singlephase input mode, connect either of them. If phase-Z is not used, the input need not be connected.

For differential line receiver input mode, you can select whether to insert the terminal resistor.

Detailed description of differential line receiver input circuit



Input signal



t_{PWH} : High-level clock pulse width 50nsec (Min.)
t_{PWL} : Low-level clock pulse width 50nsec (Min.)

⚠ CAUTION

In the input pin+, TTL level input circuit is parallel-connected.

Please use the shielded cable with a length of less than 30m to meet "CE EMC Directive".

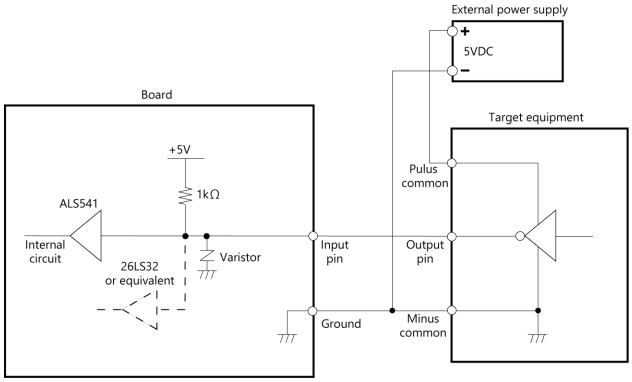
Connection Method to the External device -TTL-Level Input-

Connecting the TTL level input

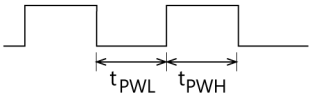
Use the TTL level -compatible input to connect the board to the TTL level -compatible output circuit of a rotary encoder or linear scale. The maximum input frequency is 10 MHz.

For use in two-phase input mode, connect both of the phase-A and phase-B inputs. For use in single-phase input mode, connect either of them. If phase-Z is not used, the input need not be connected.

Detailed description of TTL level input circuit



Input signal



t_{PWH} : High-level clock pulse width 50nsec (Min.)
t_{PWL} : Low-level clock pulse width 50nsec (Min.)

⚠ CAUTION

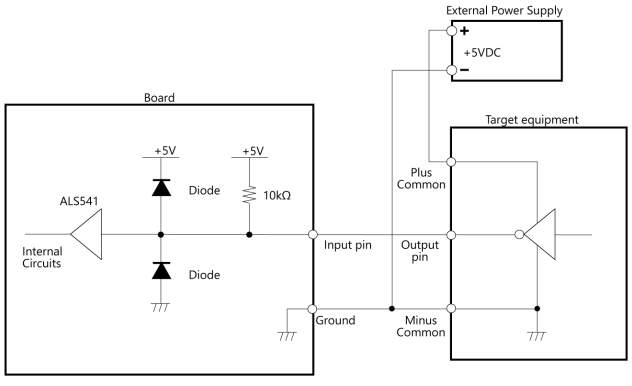
- The connection cable length should be within 1.5 m.
- To prevent malfunction caused by noise, separate the circuit as much as possible from other signal cables and noise sources.
- In the input pin+, TTL level input circuit is parallel-connected.
- Please use the shielded cable to meet "CE EMC Directive".

Connecting the control signal input/outpu

Connection of a control input

For control signal input, the board has one pin per channel to be used to selectively start/stop or preset the counter for the channel and one pin per channel to be used to start or stop the sampling clock.

Control input circuit and its sample connection



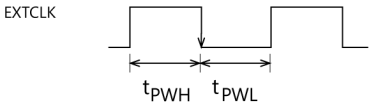
⚠ CAUTION

- The connection cable length should be within 1.5 m.
- To prevent malfunction caused by noise, separate the circuit as much as possible from other signal cables and noise sources.

- Please use the shielded cable to meet "CE EMC Directive".

External sampling clock signal (EXTCLK)

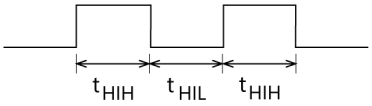
This pin feeds the external pacer clock signal. The maximum frequency is 10 MHz . When the sampling clock input has been set to the external clock input, sampling is performed at the falling edge of the signal at this pin.



t_{PWH} : High-level clock pulse width 50nsec (Min.)
t_{PWL} : Low-level clock pulse width 50nsec (Min.)

Other control input signals (DI0 - DI7, EXTSTART, EXTSTOP)

These signals are TTL level compatible and the trigger edge is software-programmable at either the rising or falling edge. High- and low-level hold times of at least 50nsec are required to detect an edge of the signal.



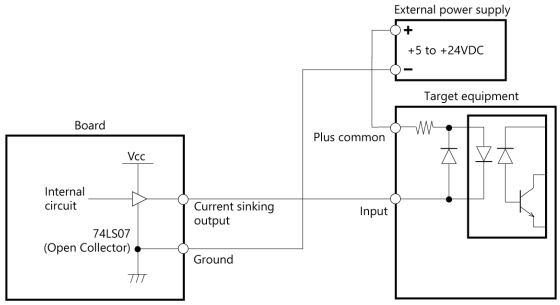
t_{HIH} : High-level hold time 50nsec (Min.)
t_{HIL} : Low-level hold time 50nsec (Min.)

Connection of a control output

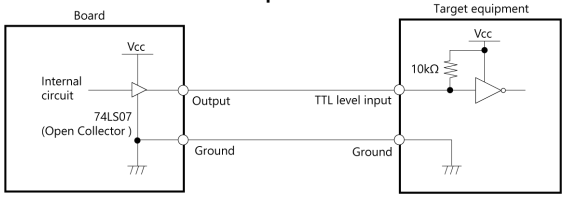
The control output of the board provides the general-purpose output signal (level output) and the one-shot pulse signals that indicate hardware events such as a count match. For the signal output, positive or negative logic can be selected with SW2.

Control output circuit and its sample connection

Sample connection to Isolated input circuit



Sample connection to TTL level input circuit



⚠ CAUTION

The output of this board has no surge voltage protector. To drive an inductive load such as a relay or lamp using this board, apply surge voltage protection to the load side. For surge voltage protection, see "Surge Voltage Countermeasures" in the next section.

Circuit Block Diagram