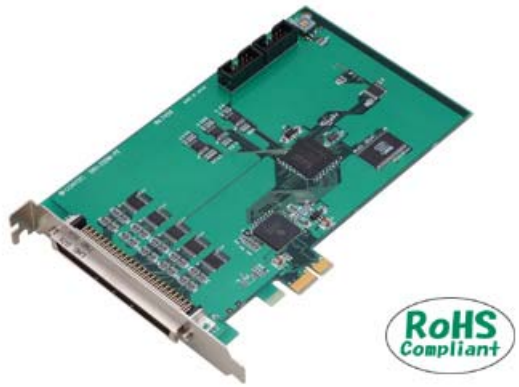
High Speed Bi-directional
Digital I/O Board for PCI Express

DIO-32DM-PE



* Specifications, color and design of the products are subject to change without notice.

This product is a PCI Express bus-compliant interface board that supports transfer by bus mastering and performs input/output between the external device and digital signal. This product features unisolated LVTTL level (Operating voltage: 3.3V) I/O 32channels and you can select input / output in 16 units.

Bus master transfer makes it possible to sample quickly large data with transfer rate at 20MHz maximum. It can be used as a pattern generator that outputs arbitrary digital patterns at high speed. It can also be used as a general-purpose I/O board when bus mastering is not used.

Windows/Linux driver is bundled with this product.

Using the dedicated library VI-DAQ makes it possible to create each application for LabVIEW.

Features

32channels of unisolated LVTTL level I/O (32 input channels / each 16channels for I/O / 32 output channels are selected.)
This product has the 32channels (operating voltage 3.3VDC, positive logic) of unisolated LVTTL level I/O whose response speed is 50nsec. They can be used for 32bit input, 16bit input plus 16bit output, or for 32bit output. Other than I/O bit, this product has the control signal (clock, start, stop and handshake signal (REQ, ACK) that can control starting and stopping the sampling (input) / generating (output)).

Sampling and generating with transfer rate at 20MHz maximum
Bus master transfer makes it possible to sample (input) or generate (output) large data with transfer rate at 20MHz maximum. As the sampling and generating features have their own bus mastering blocks each made up of two independent channels, the board can generate 16 signals while sampling 16 signals.

A synchronization control connector is provided for synchronized control of multiple boards.
A synchronization control connector is provided for synchronized control of up to 16 boards. It is also easy to synchronize operation with other CONTEC boards that have a synchronization control connector.

You can use Max. 4 input signals as interrupt request signals at the time of using the general-purpose I/O.
You can use Max. 4 input signals as interrupt request signals and also disable or enable the interrupt in bit units at the time of using the general-purpose I/O.

Windows/Linux compatible driver libraries are attached.
Using the attached driver library API-PAC(W32) makes it possible to create applications of Windows/Linux. In addition, a diagnostic program by which the operations of hardware can be checked is provided.

Functions and connectors are compatible with PCI compatible board PIO-32DM(PCI).
The functions same with PCI compatible board PIO-32DM(PCI) are provided. In addition, as there is compatibility in terms of connector shape and pin assignments, it is easy to migrate from the existing system.

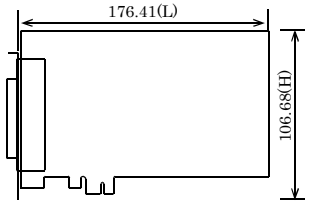
LabVIEW is supported by a plug-in of dedicated library VI-DAQ.
Using the dedicated library VI-DAQ makes it possible to create each application for LabVIEW.

Specification

Encoder Input Section

Item	Specification
Digital section	
Number of I/O Channels	32channels (select input 32channels / I/O each 16channels / output 32 channels by software)
I/O circuit	
Operating voltage	3.3VDC
Built-in power	None
Input section	
Input format	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled
Interrupt	<When general-purpose I/O is used> 4 interrupt input signals are arranged into a single output of interrupt signal INTA. An interrupt is generated at the rising edge (LOW-to-HIGH transition).
Pull-up resistor	10kΩ
Output section	
Output format	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic)
Rating (Max.)	3.3VDC 8mA
Response time	50nsec
Data access method	General-purpose digital I/O or I/O with bus master transfer
Echo-back function	Available (at general-purpose output)
Pattern input	
Sampling start trigger	Software start/External start/Pattern match/SC connector
Sampling stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Sampling clock	Sampling timer/External clock input/handshake/SC connector
Sampling timer	50ns - 107s, 25ns unit
Pattern output	
Generating start trigger	Software start/External start/SC connector
Generating stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Generating clock	Output timer/External clock input/Handshake/SC connector
Generating timer	50ns - 107s, 25ns unit
Control signal	
I/O signal level	Unisolated LVTTL level * 5V TTL level input enabled
REQ signal (handshake)	Negative logic t_L=50ns (Min.)
ACK signal (handshake)	Negative logic t_L=50ns (Min.)
External start signal	Selection of rising/falling edge with the software
External stop signal	Selection of rising/falling edge with the software
External clock input	f=10 MHz (Max.)
Bus master section	
DMA channels	2channels (one each for input and output)
Transfer bus width	32/16bit width
Transfer data length	8 PCI data length (Max.)
Transfer rate	80 MB/sec.
FIFO	1K data/ch.
Scatter/Gather function	64 MB/ch.
Synchronization section	
Control output signal	Selection of output signal with the software when specifying a sync master board.
Control input signal	Selection of sync factor with the software when specifying sync slave boards.
Max. board count for connection	16 boards including the master board
Common section	
Allowable distance of signal extension	1.5m (dependent on wiring environment)
I/O addresses	Occupies 2 locations, any 32-ports and 64-ports boundary
Current consumption	3.3V 400mA (Max.)
Operating conditions	0 - 50°C, 10 - 90%RH (No condensation)
Bus specification	PCI Express Base Specification Rev.1.0a x1
Physical dimensions (mm)	176.41(L) x 106.68(H)
Connector	PCR-E96LMD+equivalence to it [mfd. by HONDA TSUSHIN KOGYO CO., LTD.]
Weight	130g

External Board Dimensions



The standard outside dimensions (L) is the distance from the end of the board to the outer surface of the slot cover.

Differences in Bus Master Transfer Rate by System Configuration

When Fitted in the PC Expansion Slot

	Limited		Unlimited	
	In	Out	In	Out
Athlon 3800+ 2.0GHz	20	20	13.4	3.4
Core 2 Duo 2.0MHz	20	20	13.4	3.1
Pentium E2160 1.8GHz	20	20	13.4	3.1

Unit [MHz]

"Limited" indicates that the number of transfers is designated and "unlimited" indicates the number of transfers is not designated. However, these values may not be satisfied depending on the system configuration, such as other boards and applications.

When CONTEC's Expansion Unit ECH-PE-CE Series Is Used

	Limited		Unlimited	
	In	Out	In	Out
Athlon 3800+ 2.0GHz	20	20	13.4	3.1
Core 2 Duo 2.0MHz	20	20	13.4	2.7
Pentium E2160 1.8GHz	20	20	13.4	2.7

Unit [MHz]

"Limited" indicates that the number of transfers is designated and "unlimited" indicates the number of transfers is not designated. However, these values may not be satisfied depending on the system configuration, such as other boards and applications.

Support Software

Windows version of digital I/O driver API-DIO(WDM) / API-DIO(98/PC)
[Stored on the bundled CD-ROM driver library API-PAC(W32)]

The API-DIO(WDM) is the Windows version driver library software that provides products in the form of Win32 API functions (DLL). Various sample programs such as Visual Basic and Visual C++, etc and diagnostic program *1 useful for checking operation is provided.

< Operating environment >

OS	Windows Vista, XP, Server 2003, 2000
Adaptation language	Visual Basic, Visual C++, Visual C#, Delphi, C++ Builder

For more details on the supported OS, applicable language and how to download the updated version, please visit the CONTEC's Web site (http://www.contec.com/apipac/).

*1 For API-DIO(98/PC), check the device operation by using the sample program.

Linux version of digital I/O driver API-DIO(LNX)
[Stored on the bundled CD-ROM driver library API-PAC(W32)]

The API-DIO(LNX) is the Linux version driver software which provides device drivers (modules) by shared library and kernel version. Various sample programs of gcc are provided.

< Operating environment >

OS	RedHatLinux, TurboLinux (For details on supported distributions, refer to Help available after installation.)
Adaptation language	gcc

For more details on the supported OS, applicable language and how to download the updated version, please visit the CONTEC's Web site (http://www.contec.com/apipac/).

Data acquisition VI library for LabVIEW
VI-DAQ (Available for downloading (free of charge) from the CONTEC web site.)

This is a VI library to use in National Instruments LabVIEW. VI-DAQ is created with a function form similar to that of LabVIEW's Data Acquisition VI, allowing you to use various devices without complicated settings.
See http://www.contec.com/vidaq/ for details and download of VI-DAQ.

Cable & Connector

Cable (Option)

Shield Cable with 96-Pin
Half-Pitch Connectors at Both Ends : PCB96PS-0.5P (0.5m)
: PCB96PS-1.5P (1.5m)

Flat Cable with 96-Pin
Half-Pitch Connectors at Both Ends : PCB96P-1.5 (1.5m)

Shield Cable with 96-Pin
D-SUB Connector at One End : PCA96PS-0.5P (0.5m)
: PCA96PS-1.5P (1.5m)

Flat Cable with 96-Pin
Half-Pitch Connectors at One End : PCA96P-1.5 (1.5m)

Connector (Option)

Half Pitch 96P Female Connector Set
(5 Pieces) : CN5-H96F

Accessories

Accessories (Option)

Screw Terminal Unit (M3 x 96P) : EPD-96A *1*2
Screw Terminal Unit (M3.5 x 96P) : EPD-96 *1
Terminal Unit for Cables (M2.5 x 96P) : DTP-64(PC) *1

*1 PCB96P or PCB96PS optional cable is required separately.
*2 "Spring-up" type terminal is used to prevent terminal screws from falling off.

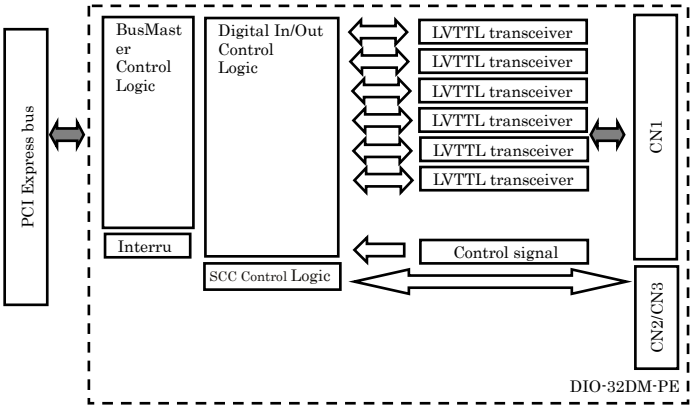
* Check the CONTEC's Web site for more information on these options.

Packing List

Board [DIO-32DM-PE] …1
SC Cable(10cm) …1
First step guide …1
CD-ROM *1 [API-PAC(W32)] …1

*1 The CD-ROM contains the driver software and User's Guide.

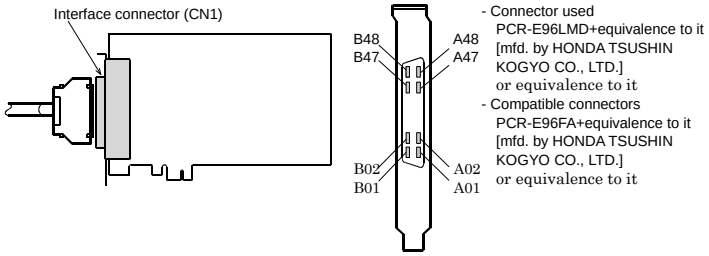
Block Diagram



How to connect the connectors

Connector shape

To connect an external device to this product, plug the cable from the device into the interface connector (CN1) shown below.



* Please refer to page 2 for more information on the supported cable and accessories.

Connector Pin Assignment

GND	B48		A48	GND
GND	B47		A47	GND
GND	B46		A46	GND
EXTCLK1	B45		A45	EXTCLK0
GND	B44		A44	GND
EXTSTART1	B43		A43	EXTSTART0
GND	B42		A42	GND
EXTSTOP1	B41		A41	EXTSTOP0
GND	B40		A40	GND
EXTREQ1	B39		A39	EXTREQ0
GND	B38		A38	GND
EXTACK1	B37		A37	EXTACK0
GND	B36		A36	GND
GND	B35		A35	GND
GND	B34		A34	GND
DIOD07	B33		A33	DIOB07
GND	B32		A32	GND
DIOD06	B31		A31	DIOB06
GND	B30		A30	GND
DIOD05	B29		A29	DIOB05
GND	B28		A28	GND
DIOD04	B27		A27	DIOB04
GND	B26		A26	GND
DIOD03	B25		A25	DIOB03
GND	B24		A24	GND
DIOD02	B23		A23	DIOB02
GND	B22		A22	GND
DIOD01	B21		A21	DIOB01
GND	B20		A20	GND
DIOD00	B19		A19	DIOB00
GND	B18		A18	GND
DIOC07	B17		A17	DIOA07
GND	B16		A16	GND
DIOC06	B15		A15	DIOA06
GND	B14		A14	GND
DIOC05	B13		A13	DIOA05
GND	B12		A12	GND
DIOC04	B11		A11	DIOA04
GND	B10		A10	GND
DIOC03	B09		A09	DIOA03 *
GND	B08		A08	GND
DIOC02	B07		A07	DIOA02 *
GND	B06		A06	GND
DIOC01	B05		A05	DIOA01 *
GND	B04		A04	GND
DIOC00	B03		A03	DIOA00 *
N.C.	B02		A02	N.C.
N.C.	B01		A01	N.C.

[ ] shows the pin No. of HONDA TSUSHIN KOGYO CO., LTD. specification.

* Can be used as an interrupt signal when used as general-purpose I/O.

DIOA00 - DIOA07	I/O signal DIOA00 - DIOA07 DIOA00 - DIOA03 can be used as interrupt signal DIOIn00 - DIOIn03 at the time of general-purpose I/O..
DIOA00 - DIOA07	I/O signal DIOA00 - DIOA07
DIOB00 - DIOB07	I/O signal DIOB00 - DIOB07
DIOC00 - DIOC07	I/O signal DIOC00 - DIOC07
DIOD00 - DIOD07	I/O signal DIOD00 - DIOD07
EXTCLK0 - EXTCLK1	External clock input
EXTSTART0 - EXTSTART1	External start signal
EXTSTOP0 - EXTSTOP1	External stop signal
EXTREQ0 - EXTREQ1	REQ signal
EXTACK0 - EXTACK1	ACK signal
GND	This is connected to GND of slot.
N.C.	This pin is left unconnected.

Connection method to the external Device -Data I/O-

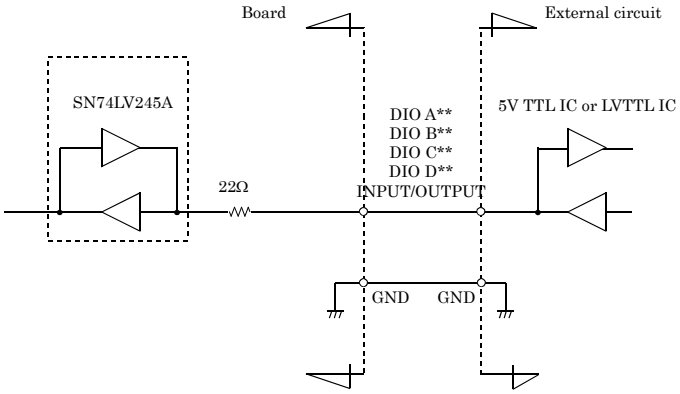
Connecting the data I/O signal(DIOA0* - DIOD0*)

These lines input from and output to external devices and can be configured in 16bit with the software.
Input and output and setting procedures are the same whether these lines are used for general-purpose digital I/O or bus master transferring and they can be configured in three different settings as shown below:

Signal name	Setup1	Setup2	Setup3
DIOA00 - DIOA07	Input	Input	Output
DIOB00 - DIOB07	Input	Input	Output
DIOC00 - DIOC07	Input	Output	Output
DIOD00 - DIOD07	Input	Output	Output

When settings 1 and 2 are used for general-purpose digital I/O, DIOA00 through DIOA03 can be used as interrupts (rising edge).

Detailed Data I/O Signal Circuit



Connection method to the external Device - Control I/O -

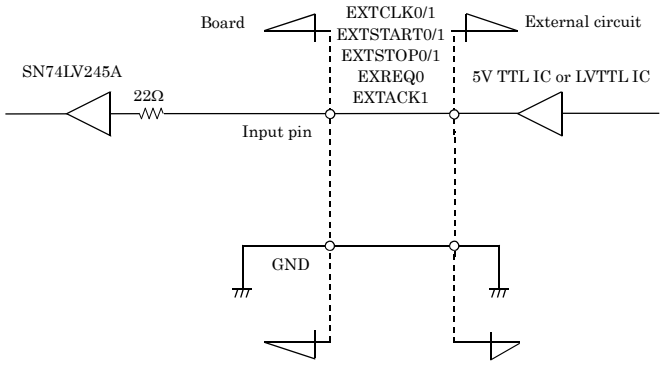
Connection to the control signal (EXT**)

In order to control bus mastering from outside, five signals are provided each for pattern I/O. Before using the signals to be input as control signals please verify their pulse widths.
"0" at the end of a signal name indicates a pattern input signal and "1" a pattern output signal.

Signal name	Direction	Usage	Signal name	Direction	Usage
EXTCLK0	In	Pattern input clock	EXTCLK1	In	Pattern output clock
EXTSTART0	In	Pattern input start signal	EXTSTART1	In	Pattern output start signal
EXTSTOP0	In	Pattern input stop signal	EXTSTOP1	In	Pattern output stop signal
EXTREQ0	In	Pattern input REQ signal	EXTREQ1	Out	Pattern output REQ signal
EXTACK0	Out	Pattern input ACK signal	EXTACK1	In	Pattern output ACK signal

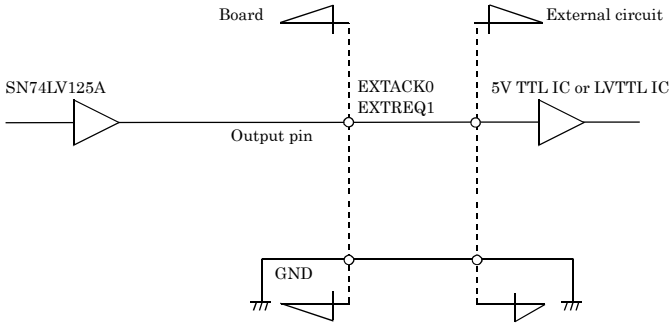
Detailed Control Input Signal Circuit

Control signals to be input include clock, start, stop, and handshake input signals.



Detailed Control Output Signal Circuit

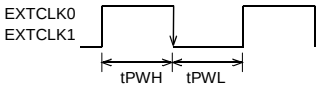
Control signals to be output include handshake output signals.



What is the Control Signal?

External clock signal (EXTCLK0/EXTCLK1)

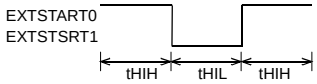
These signals input external pacer clocks. The maximum frequency is 10MHz.
When the external clock input is set as the clock source, pattern input or output occurs at the falling edge of this signal.



tPWH :	Clock pulse high width	50ns (Min.)
tPWL :	Clock pulse low width	50ns (Min.)

Eternal start signal (EXTSTART0/EXTSTART1)

These input signals start bus mastering with an external signal. The signal level is LVTTL and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.



tHIH :	High level hold time	50ns (Min.)
tHIL :	Low level hold time	50ns (Min.)

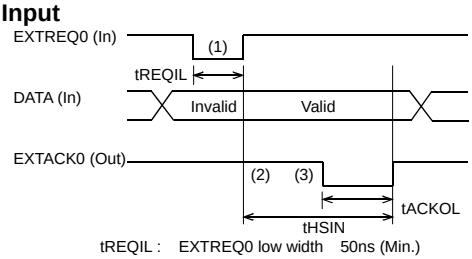
External stop signal (EXTSTOP0/EXTSTOP1)

These input signals stop bus mastering with an external signal. The signal is LVTTL level and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.

Handshake Signal (EXTREQ0/EXTACK0/ EXTREQ1/EXTACK1)

These signals handshake with external devices. The signal is LVTTL level and controlled with negative logic.

Input



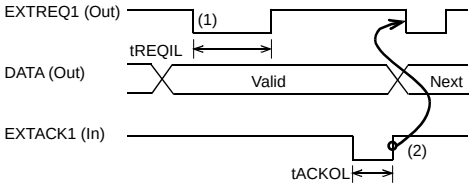
tREQIL :	EXTREQ0 low width	50ns (Min.)
tACKOL :	EXTACK0 low width	100ns
tHSIN :	Handshaking time	100ns (Min.)

(1) After setting the handshaking operation, this product samples the EXTREQ0 signal and starts pattern input when it recognizes a low pulse of more than 50ns. Pattern data prior to that time is disabled.

(2) The board generates a cycle to write data input from an external device to the PC memory by bus mastering.

(3) At the end of writing data, the board outputs acknowledge signal EXTRACK0 to notify the external device.

Output



tREQOL :	EXTREQ1 low width	100ns
tACKOL :	EXTACK1 low width	50ns (Min.)

(1) After setting the handshaking operation, this product outputs the EXTREQ1 signal.

(2) The board begins sampling acknowledge signals from external devices. The board recognizes the end with a low pulse of more than 100ns and, at the leading edge, starts preparing to output the next data.

Differences between DIO-32DM-PE and PIO-32DM(PCI)

	DIO-32DM-PE	PIO-32DM(PCI)
Input format	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled	Unisolated TTL level (Equivalent to 74ALS245A) (positive logic)
Output format	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic)	Unisolated TTL level (Equivalent to 74ALS245A) (positive logic)
Control signal	Unisolated LVTTL level (Equivalent to 74LV245A) Unisolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled	Unisolated TTL level (Equivalent to 74ALS245A) Unisolated TTL level (Equivalent to 74LS125A)
Bus specification	PCI Express Base Specification Rev.1.0a x1	PCI(32bit, 33MHz, Universal key shapes supported)
Operating voltage	3.3V 400mA (Max.)	5V 700mA (Max.)